PHASE ALIGNMENT OF DATA TO CLOCK

Abstract of the Disclosure

A phase alignment circuit in a serial transmitter aligns a parallel input data stream to a first transmission clock before conversion to a serial output data stream using a second transmission clock which is a multiple of the first transmission clock. The phase alignment circuit introduces less delay, i.e., the output of the phase alignment circuit lags the input of the phase alignment by a few number of clock cycles (e.g., less than 2 clock cycles). The phase alignment circuit demultiplexes the input data stream into a plurality of intermediate data streams using a plurality of multi-phase clocks referenced to a data clock and multiplexes the plurality of intermediate data streams using sequence signals referenced to the first transmission clock. The sequence signals are initialized according to a reset condition and at least one of the multi-phase clocks.